REMARKS/ARGUMENTS

Interview After Final

Today, the Examiner granted an interview to discuss the below rejection. Applicant explained the below argument in greater detail so as to explain that the claimed invention could accomplish more of the matrix transpose process than could Sidwell in the same amount of instructions. No final agreement was sought and none was reached. As interviews after final are discretionary, the Applicant especially appreciates this opportunity.

35 U.S.C. §102 Rejection, Sidwell et al.

The Examiner has rejected claims 1-18 and 20-22 under 35 U.S.C. §102(b) as being anticipated by Sidwell et al. (U.S. Patent No. 5,875,355). In their current form, claims 1, 9 and 17 are believed to distinguish Sidwell. More specifically, Sidwell cannot be relied on to teach or suggest: (1) starting with a matrix and storing a row or column of the transposed matrix in a first or second destinations as a result of a single instruction issue as required by claim 1; (2) a first processing path coupled to the first through fourth source registers as required by claim 9; or (3) having a plurality of sub-instructions in the same issue that process a matrix as required by claim 17. A quick word search for the terms "VLIW," "instruction word," "long instruction," or "issue" in Sidwell et al. yielded no matches in this reference. Applicant's respectfully request that the anticipation rejection be withdrawn for these reasons.

First Missing Limitation: Transpose Matrix Row/Column from Single Issue

Claim 1 requires starting with a matrix and storing a row or column of the transposed matrix in a first or second destinations as a result of a single instruction issue. Sidwell requires multiple instruction issues that are executed in serial fashion to accomplish the same feat as the claimed invention. Sidwell, Figs. 14 and 15; and Annexe A. Simply, Sidwell requires four instruction issues to complete what the claimed invention can accomplish in two, in one embodiment. Compare Sidwell, Annexe A, Sequence (i) with Application, Figs. 6A and 6B.

Second Missing Limitation: Four Input Registers Coupled to a Processing Path

Claim 9 requires coupling a first processing path to the first through fourth source registers. Sidwell only allows for one, two or three input operands. Sidwell, col. 4, lines 9-1. Four source registers allow the processing path to process larger portions of a matrix, for example.

Third Missing Limitation: Matrix Sub-Instructions in Same Issue

Claim 17 requires having a plurality of sub-instructions in the same issue that process a matrix. Sidwell can only issue a single instruction at a time. Specifically, the type unit **192** only receives a single opcode **160** and decodes it to determine what single instruction was requested. Sidwell, col. 9, lines 35-37. By processing multiple sub-instructions in a single issue, the claimed invention can perform, for example, a matrix transpose of a 4x4 matrix where each input register holds four elements with two multi-word instructions. Sidwell requires four instruction issues to accomplish the same transpose. Sidwell, Figs. 14 and 15; and Annexe A.

For at least these reasons, the Applicants respectfully request reconsideration of the rejection to claims 1-18 and 20-22.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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